Data Communication

By
Edward Cheung
email: icec@polyu.edu.hk
15 July, 2003.

Agenda

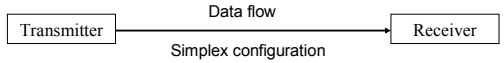
- **Transmission Mode**
- **Channel Capacity**
- **Nyquist Theorem**
- **Hartley-Shannon's Theorem**
- **Synchronization in Telecommunication Systems**
- **Synchronous and Asynchronous Data Communication**
- **Modem**
- **Packets**
- **Frames**
- **Error Detection**

Introduction

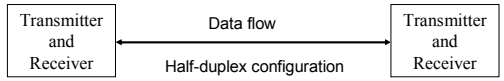
- Voice Communications is the the movement of voice traffic between telephones.
- Data Communications is the movement of data between computers.
- Modern computers are referred to as digital computers because their internal operation relies on digital signaling.

Transmission Mode(1)

- Simplex Mode
  - Data is passed in one direction only

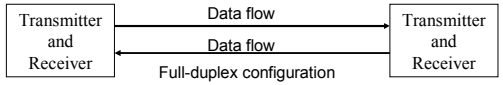


- Half-duplex Mode
  - Only one direction of transmission is active at one time



Transmission Mode(2)

- Full-duplex Mode
  - Data is passed in both directions simultaneously



- All personal computer modems and many commercial modems use full-duplex mode.
- Full-duplex transmission provide more efficient throughput.

Channel Capacity

In 1928, Hartley states that the amount of information that can be transmitted over a given channel is proportional to the product of the channel bandwidth and the time of operation and that one quantity can be traded for the other.

$$\textit{Amount of information} = const \cdot BT\log V$$

Where V is the number of current values / size of the signalling alphabet / number of states

Bandwidth is measured in ***cycles per second*** or ***Hertz*** (Hz).

Two major theories that relate to the amount of information that can be transmitted through a medium are the Nyquist Relationship and Shannon's Law.

Nyquist's Theorem

Nyquist states that the information of a sampled message can be recovered if the samples are taken at a rate which is at least twice that of the value of the highest signaling frequency.

It follows that the maximum data rate (R) in bits per second that can be achieved over a transmission system of bandwidth B is:-

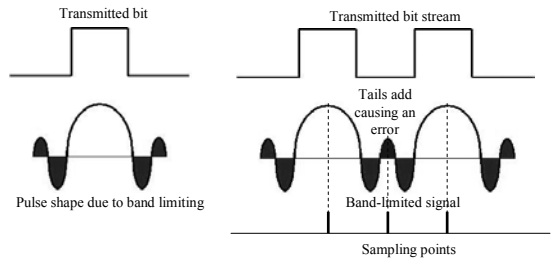
$$R = 2B\log_2 V \ \textit{bits/sec}$$

where ***B*** is the bandwidth and ***V*** is the number of discrete state.

For noiseless voice-grade telephone circuit with 2-level binary signal, the maximum data rate = 2B = 2x3000=6kbps. Under noiseless environment, V can be infinite which implies no limit.

Intersymbol Interference

Pulse response through a band-limited channel



The bandwidth limitation of a channel causes the leading and trailing edges of a pulse to interfere with other pulses as the signal change exceeds twice the bandwidth of a channel.

Shannon's Information Capacity Theorem

Shannon's theorem is used to determine the maximum bit rate that can be used over a band-limited channel under noisy environment.

For noisy channel with signal to noise ratio S/N, the maximum channel capacity is given by

$$C = B \log_2 (1+S/N)$$

Where C = Maximum channel capacity in bps,

B= Channel bandwidth in Hz,

S = power of the transmitter,

N = power of thermal noise.

Shannon's Information Capacity Theorem (cont.)

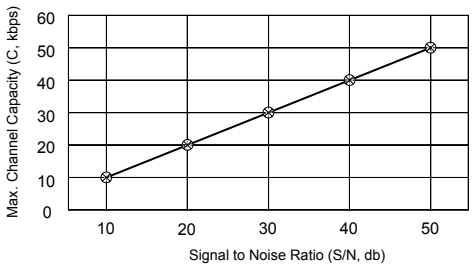
A typical analog telephone channel have a S/N ratio of 30 dB, which represents a value of 1000. The maximum data transmission capacity thus becames

$$C = B \log_2 (1+S/N)$$
$$= 3000 \log_2 (1 + 1000)$$
$$= 3000 \log_2 (1001)$$
$$= 3000 \times 10 \text{ (approximately)}$$
$$= 30\,000 \text{ bps}$$

This is the theoretical limit on Gaussian noise channel that the data can be transmitted without error.

Shannon's Information Capacity Theorem (cont.)

We can evaluate the maximum channel capacity for a voice-band channel with a bandwidth of 3000 Hz. We can obtain an approximately straight line relationship.



Shannon's Channel Coding Theorem

Channel noise does not limit the accuracy of communication. It only limits the rate which information can be reliably transmitted.

It is not possible to transmit at a rate higher than C bps by any encoding system without a definite probability of error.

The channel capacity theorem defines the fundamental limit on the rate of error-free transmission for a power-limited, band-limited Gaussian channel. The theorem also known as the Hartley-Shannon Law. Under Gaussian noise of power spectral density $N_o/2$ and average transmitting power P

$$C = B \log_2 (1+P/N_oB) \text{ bps}$$

Synchronization

The coherent reception of a digitally modulated signal requires that the receiver be synchronous to the transmitter.

Two basic modes in digital communication systems:-

- Carrier synchronization
  - Estimation of carrier phase and frequency
  - Carrier recovery for coherent detection
- Symbol synchronization
  - Estimation of the starting and finishing times of individual symbols
  - Clock recovery

Data Link Layer

- Data are transmitted in either synchronous mode or asynchronous mode.
- Synchronous mode: symbols are sent continuously at a fixed periodic rate.
- Asynchronous mode: stream of data bits is broken into a number of words, typically made up of a start bit, 8 data bits, a optional parity bit and a stop bit. The transmission interval between words is irregular.
- In either mode of transmission, it is necessary that the received symbol is sampled at the right time – symbol synchronization.
- Either the transmitter clock or the receiver clock is needed for synchronous transmission.

Data Link Protocols

- Asynchronous Protocols
  - Xmodem
  - Ymodem
  - Zmodem
  - Kermit
- Synchronous Protocols
  - Character-oriented Protocols
    - Binary Synchronous (Bi-Sync) – IBM
    - Point-to-Point (PPP)
  - Bit-oriented Protocols
    - Synchronous Data Link Control (SDLC) – IBM
    - High-level Data Link Control (HDLC) – ISO

Asynchronous Transmission (1)

In asynchronous transmission, each character to be transmitted is encoded into a series of pulses.

The transmission of the character is started by a start pulse equal in length to a code pulse.

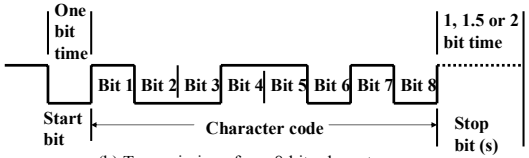
The encoded character (series of pulses) is followed by one or two stop pulses.

Each end unit has a baud rate generator and they are synchronized by the start bit.

Asynchronous Transmission (2)

STB: start bit
CB: character bit
SPB: stop bit

(a) Idle time between character transmission.



(b) Transmission of one 8-bits character

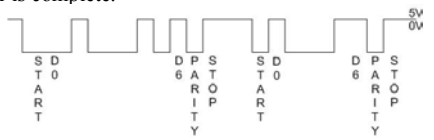
Asynchronous Transmission (3)

The start bit represented a transition from a mark to a space.

No data are transmitted the line is held in a 'mark' condition.

The START bit serves as an indicator to the receiving device that a character of data follows.

The STOP bit causes the line to be placed back into its pervious 'marking' condition, signifying to the receiver that the data character is complete.



Asynchronous Transmission Characteristics

1. Each character is prefixed by a start bit and followed by one or more stop bit. Thus, the complete transmission requires a minimum of nine bits.
2. Idle time (period of inactivity) can exist between transmitted characters.
3. Bits within a character are transmitted at prescribed time intervals.
4. Timing is established independently in the computer and terminal. No synchronization between sender and receiver; no carry-on clock signal.
5. Good for low speed connection; e.g. terminal monitor.

Example – Serial Port RS-232

- RS-232 is a popular standard used for asynchronous communication and it is equipped in PC. Other examples of asynchronous adapters are RS422 & RS485.
- The RS232 was established in 1960 by Electronic Industry Association (EIA)
  - Current version is RS-232-E published in 1991
  - In this version, EIA only change the prefix from RS to EIA

RS-232

There are 4 aspects to the RS232 standard

- Electrical specifications
  - Specifies the voltage level, rise time, fall time of each signal, achievable data rate and the distance of transmission
- Functional specifications
  - Function of each signal
- Mechanical specifications
  - The number of pins and the shape and dimension of connectors
- Procedural specifications
  - Sequence of events for transmitting data, based on the functional specification of the interface

RS-232

The RS-232 standard specified the electrical and mechanical characteristics of the connection.

Connect Data Terminal Equipment (DTE); e.g. PC and Data Communication Equipment (DCE); e.g. modem.

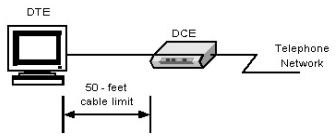
Connecting a RS-232 Link needs:-

- Baud rate; Bit pattern, the parity (Odd/Even/None), the number of Stop Bits; Flow control.

RS-232

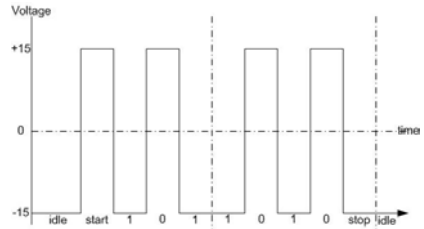
RS-232 standards apply to series data transfers between a DTE and DCE in the range from 0 to 19.2kbps. For short distance, RS-232 can operate at 33.6kbps. Typical terminal setting is 9600bps.

The standards limit the cable length between a DTE and DCE to 50 feet.



RS-232 allows a sender to transmit a character at any time and to delay arbitrarily long before sending another.

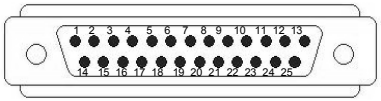
RS232 Signal



- Negative logic; -15 V to represent a binary 1 (mark), and
- +15 V to represent a binary 0 (space).
- Tolerance input (0/1) :+3V to +25V / -3V to -25V
- Tolerance output (0/1) : +5V to +15V / -3V to -15V

RS232 Connector

RS-232 interface specifies 25 interchange circuit or conductors that govern the data flow between the DCE and DTE



Pin No.
1 : Protective Ground
2 : Transmitted Data
3 : Received Data
4 : Request to Send
5 : Clear to Send
6 : Data Set Ready

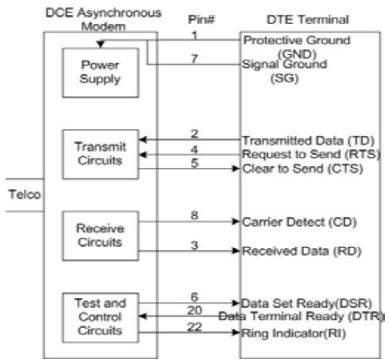
Pin No.
7 : Signal Ground
8 : Carrier Detect
18 : Local Loop Back
20 : Data Terminal Ready
22 : Ring Indicator
25 : Busy

RS-232 Connector Conversion

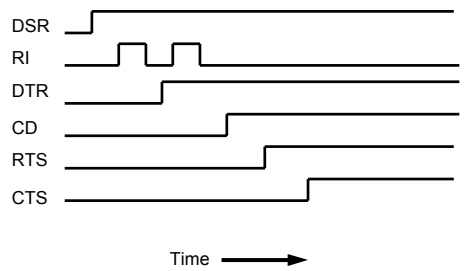
A list of corresponding pins between a DB-9 connector used on an IBM PC serial port and a standard RS-232 DB-25 connector.

DB-9		DB-25
1	Carrier Detect	8
2	Receive Data	3
3	Transmitted Data	2
4	Data Terminal Ready	20
5	Signal Ground	7
6	Data Set Ready	6
7	Request to Send	4
8	Clear to Send	5
9	Ring Indicator	22

Connection between a DCE and a DTE using RS-232



RS-232 Control Signal Timing



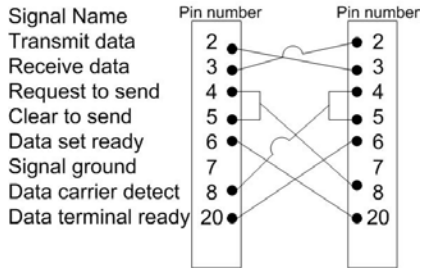
The state of the control signals varies in time and existence as depending upon the operation characteristics of devices connected as well as the optional settings of those devices.

RS-232 Control Signal Timing

1. Data set is powered, the Data Set Ready (DSR) control signal being high or in the ON state.
2. Two Ring Indicator (RI) signals are passed to the computer port, resulting in the computer responding by raising its Data Terminal Ready (DTR) signal.
3. The DTR signal in conjunction with the second Ring Indicator (RI) signal results in the modem answering the call.
4. The Carrier Detect (CD) signal to the computer port. Assuming that the computer is programmed to transmit a sign-on message, it will raise its Request to Send (RTS) signal.
5. The modem will respond by raising its Clear to Send (CTS) signal if it is ready to transmit, which enables the computer port to begin the actual transmission of data.

Connecting DTE Back-to-back using RS-232

A null modem is a special cable that is designed to eliminate the requirement for modems when interconnecting two collocated data terminal equipment devices.



The RS-232 Null Modem

- The cable configuration will work for most data terminal equipment with handshaking flow control.
- Exception is that when a terminal device is to be cabled to a port on a mainframe computer that operates the terminal as a 'ring-start' port. In this situation, the null modem may be modified so that Data Set Ready (DSR, pin 6) is jumpered to Ring Indicator (RI, pin 22) at the other end of the cable to initiate a connect sequence to a 'ring-start' system

Full Duplex Asynchronous Connection

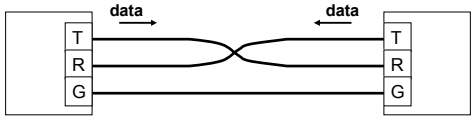
In RS-232 applications, data must flow in two directions at the same time. Simultaneous transfer in two directions is known as ***full duplex transmission.***

Full duplex transmission RS-232 requires a wire for data traveling in one direction, a wire for data traveling in the reverse direction, and a single ground wire used to complete the electrical path in both directions.

As long as it remains capable of receiving characters, a receiver supplies voltage on one of the control wires, which the sender interprets as ***clear to send***.

Minimum Wiring for Serial Port / Null Modem

To reduce costs, RS-232 is flexible and the device can be configured to ignore the control wires and assume the other end is working. For full duplex connections only require three wires. (two for the data signals traveling in each direction and a common ground for completing the circuit)



Baud Rate and Framing Error

Baud Rate:

To make RS-232 hardware, manufacturers usually design each piece of hardware to operate at a variety of baud rates. The baud rate can be configured, either manually or automatically.

If the sending and receiving hardware are not configured to use the same baud rate, errors will occur due to out of synchronization. To detect errors, a receiver measures the voltage for each bit multiple times (16 times of data rate) and compares the measurements. If the voltages do not all agree or if the stop bit does not occur exactly at the time expected, the receiver reports an error. Such errors are called ***framing errors.***

Common Errors in Asynchronous Serial Link

- Framing Error
  - A framing error occurs when a received character is improperly framed by the start and stop bits; it is detected by the absence of the stop bit. This error indicates a synchronization problem, faulty transmission or a break condition.
- Receiver Overrun
  - One or more characters in the data stream were received but were not read from the buffer before subsequent characters were received.
- Parity Error
  - A parity error occurs when an odd number of bits change value. It can be detected by a parity error detection circuit.

Application of Framing Error

Framing Error:

RS-232 hardware can make use of framing errors in terminal monitor application.

ASCII keyboards include a *BREAK* key but pressing *BREAK* key does not generate an ASCII code. When a user presses *BREAK,* the keyboard places the outgoing connection in a 0 state much longer than it takes to send a single character. A frame error is generated and the system can handle the error accordingly; for example, abort operation, clearing buffer and initialize the keyboard.

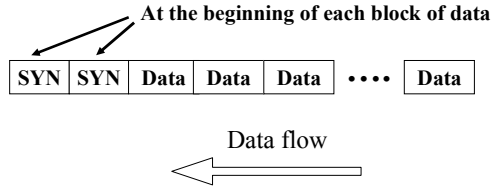
Synchronous Communication

For synchronous mode of transmission at the DTE-DCE interface, no start or stop bits preceding or following each character. This can speed up the transmission by 20% to 30%; 7 or 8 bits instead of 10 to 11 bits per character.

Data are sent in a steady, non-stop stream, blocks mode. Local and remote modems synchronize themselves by means of special framing signals that surround blocks of data. The devices connected must agree on a common clock source.

Synchronous transmission method is used as short haul modem (~4km), with V.35 interface on DB-25 or Winchester (ISO2593) connector. Speed from 2.4kbps to 128kbps depending on line condition; wiring and distance. Mainly use to connect to mainframe, replaced by modem eliminator.

Synchronous Transmission Example



In synchronous transmission, one or more SYN character (ASCII $16) can be transmitted to establish clocking prior to the transmission of data. – Frame character markers

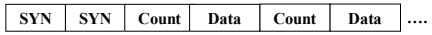
Synchronous Transmission

Synchronous Transmission technique characteristics:

1. SYN characters prefix transmitted data.
2. SYN characters are transmitted between blocks of data to maintain line synchronization.
3. No gaps exist between characters.
4. Timing is established and maintained by the transmitting and receiving modems, the terminal or other devices
5. Terminals must have buffers.
6. Transmission speeds are normally in excess of 2000 bps.

Data Link Layer

- Received raw bits from physical layer
- Need to mark the frame and control error
- If we count the number of bits by establishing a Count Field in the header, e.g.



Problem:- single bit error resulted in wrong character count and lost synchronization.

Count field alone is insufficient.

Data Link Framing

- If we add frame character markers
- Mark the beginning and end of frame with control characters.

STX	Data	ETX	STX	Data	ETX	....

Robust to bit error, synchronization lost due to bit error in frame marker can be recovered.

STX	Data	X	STX	Data	ETX	....

We can use character stuffing if there are any identical control characters in the data stream.

Synchronous Characteristics

The characteristics of synchronous transmission are:

- Data is transmitted in block. Usually, each data block is called a frame.
- The data block is needed to be synchronized between the sender and the receiver

Synchronous transmission format is ideal for high speed and high volume data.

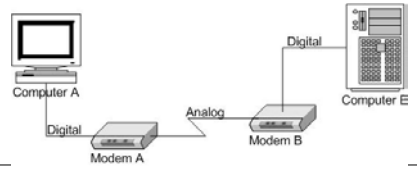
Synchronous transmission requires relatively more sophisticated hardware that precedes an entire block of data with sync characters.

Conversion Devices (1)

Characteristics of Electrical Signals:

A signal-conversion device is usually required to connect two computers

- Computer signaling is digital
- Communication channels use analog signaling



Modulation

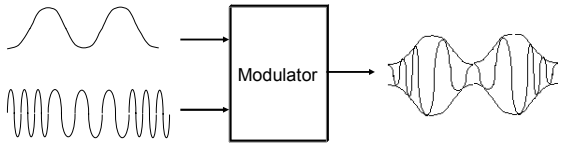


Figure: Signal Modulated

- Modulation is a process where two input signals :
  - A constant carrier frequency signal
  - a variable signal that carries the frequency information
- Two signal are combine to produce a unique output signal.

Modulation Process

- For analog signal,
  - The carrier is normally a sine wave, represented by

$$a = A \sin(2\pi ft + \phi)$$

Where **a** = instantaneous value of voltage at time t

A= maximum amplitude,

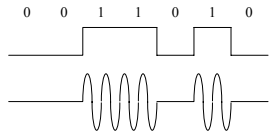
f = frequency

ϕ = phase

- The carrier's amplitude for amplitude modulation (AM).
- The carrier's frequency for frequency modulation (FM).
- The carrier's phase angle for phase modulation (PM).

Amplitude Modulation

- The simplest method of modulation is amplitude modulation(AM)
- The amplitude of a signal refers to the magnitude of the size of the signal, measured as the peak-to-peak voltage of the carrier signal



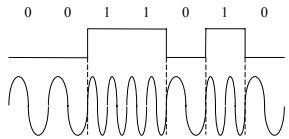
Amplitude Keying Modulation (AFK)

Amplitude Modulation

- The main application for AM is in carrier telephony, specifically the frequency division multiplex (FDM) system.
- Amplitude modulation is used in the form of AM radio and television signals.
- Advantage of amplitude modulation:
  - The simplicity of the receiver demodulation circuit
  - Simple demodulation by low-pass filter.

Frequency Modulation

- Frequency modulation (FM) is also relatively simple modulation technique
- FM translates the digital 0s and 1s into two pre-assigned discrete frequencies.



Frequency Shift Keying (FSK) Modulation

Frequency Modulation

- Frequency modulation was used in the design of low-speed acoustic couplers and modem.
- The transmitter shifted form one frequency to another as the input digital data changed form a binary 1 to a binary 0 or from a 0 to a 1. This shifting in frequency is known as ***frequency shift keying*** (FSK).
- The amplitude of an FSK signal remains constant, but its frequency changes from a mark to a space, and vice versa.

Phase Modulation

- Phase modulation is the process of varying the carrier signal with respect to the origination of its cycle.
- Phase is the position of the waveform of a signal

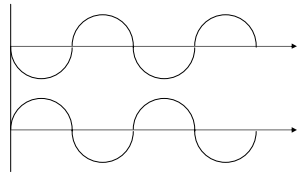
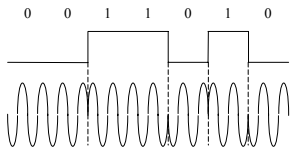


Figure: Phase modulation

Phase Modulation

- Phase modulation / Phase-shift keying (PSK), the transmitter shifts the phase of the carrier signal to represent each bit entering the modem.
- The two-phase modulation where a 180° phase change is used to inform the receiver of a change in the value of the modulated bit.



Two-phase shift keying modulation (BPSK)

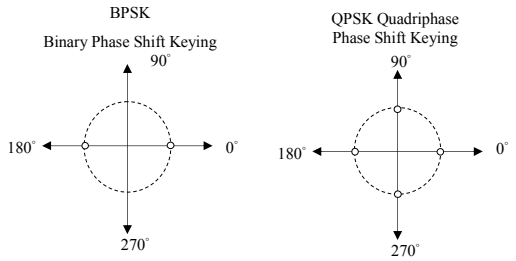
Phase Modulation

- Phase modulation relies on incremental phase changes rather than on the absolute phase value of the carrier signal
- This method to detect the transmitted signal obviates the need for keeping an absolute time standard at the transmitting and at the receiving terminals.
- Synchronization procedure is required for phase modulation techniques to ensure that the initial conditions are correct and that the received signals are properly interpreted.

Advanced Digital Modulation

- If we use 4 different phases to represent data, we can assign a group of 2-bit (dibits) per phase. We have Quadriphase-shift-keying modulation (QPSK),
- 3-bit (tribits) implies 8-PSK.
- In practise, 8-PSK is not used and use 8-QAM.
- QAM combines PSK and AM
- 8-QAM only requires 4 phases and 2 different amplitude to represent tribits.
- 16QAM uses 12phase angles and 3 amplitude levels to represent 4-bit.
  - For a modem of 2400 baud, the data rate can reach 9600bps.

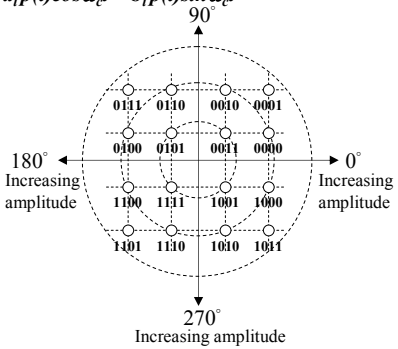
Constellation Diagram



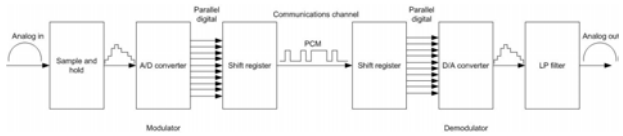
- the more bits per cycle (hertz) that are encoded, the signal will be more susceptible to interference and fading or effectively shortened the communication range

16 QAM Constellation Diagram

$$s(t) = a_i p(t)\cos\omega_c t + b_i p(t)\sin\omega_c t$$



Digital Telephone System



- Voice channel band limit from 300Hz to 3100Hz
  - Nyquist rate is 6200Hz
- Standard Sampling frequency is 8 kHz
- Time Division Multiplexing (TDM) each frame occupies 125 μ sec which consists of 24 x 8bit + 1bit synchronization = 193 bit total
- The duration of each bit is 0.647 μ sec and the resulting transmission rate is 1.544 Mbps.

CCITT Telephone Modem Characteristics (1)

The International Telecommunications Union (ITU), formerly known as the International Telegraph and Telephone Consultative Committee (CCITT),

The table shown here lists most of the standard types, showing how the complexity and number of symbol states increase as the throughput increases.

CCITT (ITU) Telephone Standards

Version no	Bit rate	Modulation format	Protocol
Bell 103	0-300	FSK	async
Bell 202	1200	FSK	async
V.22	1200/600	QPSK/FSK	async/sync
V.26bis	2400	QPSK	sync
V.27	4800/2400	8-DQPSK/ QDPSK	sync
V.29	9600	16-APK	sync
V.32	9600	32-QAM/ 16-QAM	sync
V.33	14 400	32-QAM	sync
V.34	33 600	>1024-QAM	sync
V.90	56 000	>1024-QAM	sync

Modem Handshaking (1)

- Modem handshaking is the exchange of control signals to establish a connection between two data set.
- These signals are required to set up and terminate call, and the type of signalling used is pre-determined according to one of three major standards (Electronics Industry Association):
  - RS-232 Standard
  - RS-449 Standard
  - ITU-T V.24 Recommendation.

Modem Handshaking (2)

Table: Modem handshaking signals and their function

Control signal	Function
Transmit data	Serial data sent from device to modem
Receive data	Serial data received by device
Request to send	Set by device when user program wishes to transmit
Clear to send	Set by modem when transmission may commence
Data set ready	Set by modem when it is powered on and ready to transfer data; set in response to data terminal ready
Carrier detect	Set by modem when signal present
Data terminal ready	Set by device to enable modem to answer an incoming call on a switched line; reset by adaptor disconnect call
Ring indicator	Set by modem when telephone rings

Modem Handshaking (3)

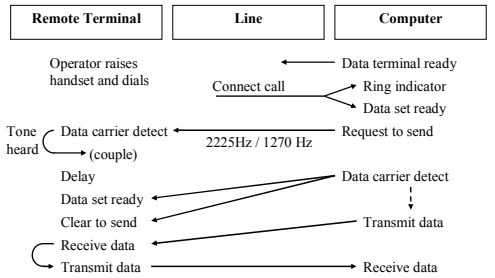


Figure: Modem handshaking Sequence

Modem Handshaking (4)

- Modems contain a series of LED indicators on the front panel of the device that display the status of the modem's operation.

Symbol	Meaning	Status
HS	High Speed	ON when the modem is communicating with another modem at 2400 baud
AA	Auto answer / Answer	ON when the modem is in auto answer mode and when on-line in answer mode
CD	Carrier detect	ON when the modem receives a carrier signal from a remote modem. Indicates that data transmission is possible
OH	Off hook	ON when the modem takes control of the phone line to establish a data link
RD	Receive data	Flashes when a data bit is received by the modem from the phone line, or when the modem is sending result codes to the terminal device
SD	Send data	Flashes when a data bit is sent by the terminal device to the modem
TR	Terminal ready	ON when the modem receives a Data Terminal Ready singal
MR	Modem ready / Power	ON when tbe modem is powered on
AL	Analog loopback	ON when the modem is an analog loopback self-test mode

ADSL Modems (1)

- Asymmetric Digital Subscriber Line (ADSL) allocates bandwidth asymmetrically in the frequency spectrum.
- ADSL is designed to provide:
  - A downstream data transfer up to 8 Mbps
  - An Upstream data transfer up to 1.5 Mbps
- An ADSL circuit with ADSL modems connected to each of a twisted-pair line has three channels:
  - A high-speed downstream channel
  - A medium -speed upstream channel
  - A standard voice telephone channel

ADSL Modems (2)

- ADSL requires the use of splitters at both the central office and the subscriber's premises to separate low and high frequencies from one to another.

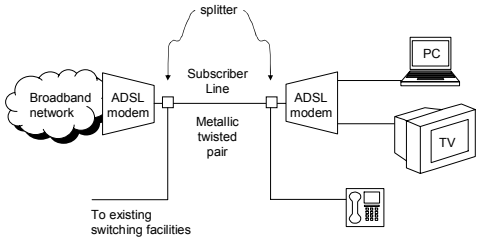


Figure : Basic operation of an ADSL circuit

ADSL Modems (3)

- The downstream operating rare depends upon the length of subscriber line, its wire gauge, the presence or absence of bridged taps and level of interference on the line.
- Line attenuation increases with line length and frequency, while it decreases as the wire diameter increases.

Table : ADSL performance

Operating rate	Wire gauge	Subscriber line distance
1.5 / 2.0 Mbps	24 AWG	18000 feet
1.5 / 2.0 Mbps	26 AWG	15000 feet
6.1 Mbps	24 AWG	12000 feet
6.1 Mbps	26 AWG	9000 feet

ADSL Operation (1)

- Two competing technologies used to provide ADSL capabilities:
  - Discrete Multi-tone (DMT) Modulation
  - Carrier-less Amplitude/Phase (CAP) Modulation
- Both DMT and CAP permit the transmission of high-speed data using Frequency division Multiplexing (FDM) to create multiple channels on twisted-pair.
- FDM frequency spectrum is partitioned into three parts.

ADSL Operation (2)

- FDM assigns one channel from 0 to 4kHz is used for normal telephone operations.
- And a second channel for upstream data.
- The third channel for downstream data for Two competing

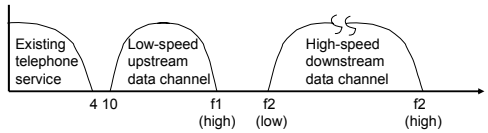


Figure : ADSL Frequency Spectrum

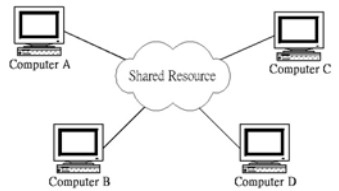
- The downstream path can be subdivided through time division multiplexing to derive several high and low speed sub-channels by time.

Concept of Packets (1)

- The network system divides data into small blocks called ***packets***, which it sends individually.
- Computer networks are often called ***packet networks*** or ***packet switching networks*** because they use packet technology.
- Two facts motivate the use of packets.
  - Small packet helps in error checking.
  - Second, communication circuits are expensive, multiple computers often share underlying connections and hardware.

Concept of Packets (2)

- A single computer can hold a shared resource only long enough to send a single packet, and must wait until other computers have a turn before sending a second packet.
- Example: Computer *A* sends a file to computer D, computers *B* and C must wait.



Frames (1)

The term "Frame" to denote the definition of a packet used with a specific type of network.

the network can use two of the un-printable ASCII characters to delimit the frame.

An example frame that uses character ***SOH*** to mark the beginning of the frame and ***EOT*** to mark the end.

SOH	block of data in frame	EOT

The format is simple and unambiguous - a receiver can tell when the entire frame has arrived, even if there are delays between characters.

Frames (2)

Disadvantage of framing scheme:

- Overhead
  - delimits both the beginning and end of each frame sends an extra, unnecessary character between blocks of data.

Advantage of framing scheme:

- Prevent large delays and computer crash
  - the reboot completed before the sender began to transmit a frame. (in which case the SOH arrives before any other characters from the frame)
  - Or the sender began to transmit before the reboot completed. (in which case the SOH will be lost, and another character will arrive first).

Transmission Error

Transmission Errors -- the problems of lost, changed, or spuriously appearing bits account for much of the complexity needed in computer networks.

Interference, such as lightning and power surges, can cause permanent damage to network equipment.

Interference can completely destroy a signal, meaning that although the sender transmits, the receiver does not detect that any data has arrived.

Error Correction

- The ability of the receiver to both detect and correct errors is known as forward error correction (FEC)
- FEC techniques are useful because they can decrease the number of retransmission required.
  - Simple parity
  - Checksum
  - CRC

Parity Bits and Parity Checking (1)

Parity bits are used on asynchronous data streams to determine whether the received data has been errored or not.

Parity check, the mechanism requires the sender to compute an additional bit, called a **parity bit**, and to attach it to each character before sending.

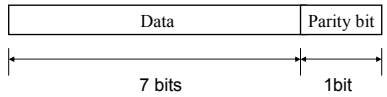
The transmitter determines the status of the parity bit and inserts it into the data stream, normally at the back of the stream.

The receiver determines what the parity should be using the data bits only and then compares this to the status of the received parity bit.

Parity Bits and Parity Checking (2)

If the two states are the same then the receiver assumes that the received data is error free.

If the two states are different then the receiver assumes that the data was in error.

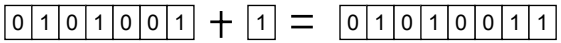


Parity Bits and Parity Checking (3)

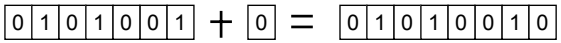
Two forms of parity, Even and Odd;

Both the sender and receiver must agree on which form is being used.

***Example: Even P*arity: total number of ones is even**



***Example: Odd P*arity: total number of ones is odd**

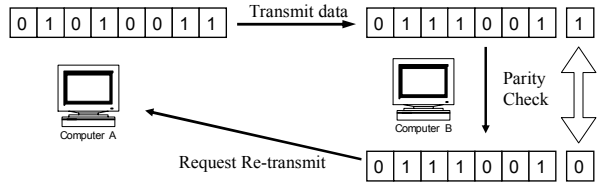


Parity Bits and Parity Checking (4)

Parity Checking:

If interference changes one of the bits during transmission, the receiver's computation will not agree with the sender and the receiver will report a parity error.

***Example: Even P*arity**



Example - Error Detection for Synchronous Transmission

Geometric Codes:
Geometric codes attack the deficiency of parity by extending the parity to two dimension-block.

This involves forming a parity bit on each individual character as well as all the characters in the block

Block parity character is also known as the "Longitudinal Redundancy Check" (LRC) character.

Error Detection – 2-dimensional Parity

		Character parity bit
Character 1	**1 0 1 1 0 1 1 0**	
Character 2	**1 1 0 0 1 0 1 0**	
Character 3	**0 1 1 0 1 0 0 1**	
Character 4	**1 0 0 1 0 0 1 0**	
Character 5	**0 1 1 1 1 0 1 0**	
Character 6	**1 0 1 0 0 0 0 1**	
Character 7	**0 1 0 1 1 1 0 1**	
Character 8	**0 1 1 1 0 0 1 1**	
"LCR"	**1 0 0 0 1 1 0 1**	

Checksum

Computer network systems send a **checksum** along with each packet to help the receiver detect errors.

Checksum is the least significant byte of the arithmetical sum of the binary data transmitted. To compute a checksum, the sender treats the data as a sequence of binary integers and computes their sum.

If the checksum at the receiver end is not identical, it is likely that an error has occurred and the receiver should request the block of data be resent.

Checksum Example

For example, Figure illustrates a 16-bit checksum computation for a small text string.

To compute a checksum, the sender treats each pair of characters as a 16-bit integer and computes the sum. If the sum grows larger than 16 bits, the carry bits are added into the final sum.

H	e	l	l	o		w	o	r	l	d	.
48	65	6C	6C	6F	20	77	6F	72	6C	64	2E

4865 + 6C6C + 6F20 + 776F + 726C + 642E + carry = 71FC

16-bit checksum computation for a string of 12 ASCII characters. Characters are grouped into 16-bit quantities, added together using l6-bit arithmetic, and the carry bits are added to the result.

Advantages and Disadvantages of using Checksum

Advantages:

- **Network that employ a checksum technique use a 16-bit or 32-bit checksum, and a signal checksum for an entire packet.**
- **The small size of the checksum implies that the cost of transmitting the checksum is small**
- **Since checksums only require addition, the computation required to create or verify a checksum is small.**

Advantages and Disadvantages of using Checksum

Disadvantages:

- Checksum is not sufficient to detect a transmission error that reverses a bit in each of four data item.
- *Example:*

	Data Item in Binary	Checksum Value	Data Item in Binary	Checksum Value
	0001	1	0011	3
	0010	2	0000	0
	0011	3	0001	1
	0001	1	0011	3
Same checksum ⇨	Total	7	Total	7

- Despite the changes, a receiver will declare that the packet has a valid checksum

Cyclic Redundancy Check

- An error code that incorporated into a data frame
- Also known as the Frame Check Sequence or the polynomial code
- Treating bit strings as representations of polynomials with coefficients of 0 and 1 only.
- Develop from algebraic field theory, polynomial arithmetic is done in modulo 2, no carries for addition or borrows for subtraction.
- Cyclic code – code word is generated by shifting and adding
- Addition and subtraction are identical to ***Exclusive Or***
- An [n,k] code C is cyclic if $x=(a_0,a_1,a_2,..,a_{n-1})$ is in C than all its cyclic e.g. $x=(a_{n-2},a_{n-1},a_0,\ldots,a_{n-3})$ are also in C.

CRC Code

- E.g. 1101 is a cyclic code than any 7-tuple of successive digits in the following code is a codeword

  1101000 1101000 1101000 1101000

  110 1000110 1000110 1000110 1000
- The idea is to append a checksum to the end of the frame such that the polynomial represented by the coded frame is divisible by G(x).
- If there is an error in the transmission, a remainder will be obtained after the division.

Benefits of CRC Error Detection

- A generator polynomial G(x) of r bits will detect;
  - All single bit error
  - All double bit error
  - All odd number of bit error
  - All burst error of length less than r+1 bits
  - $(1-1/2^{r-1})$% burst error of exactly r+1 bits in length
  - $(1-1/2^{r})$% burst error of length longer than r+1 bits

Note:

- Parity code is a special case of CRC code
- G(x)=x+1
- E.g. M(x)=[1000] => T(x)=[10001]

Requirement for CRC Error Detection

- Both sender and receiver must agree upon a generator polynomial G(x)
- m-bit transmitting data M(x) is divided by the polynomial G(x)
- The transmitting frame must be longer than G(x)
- The reminder R(x) is appended to the data and send to the receiver; i.e. M(x)+R(x)
- At the receiver end, the coded word (M(x)+R(x)) is divided by G(x) and the coded word is error free if no remainder is found.

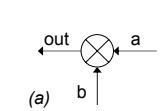
CRC Generator Polynomials

- Example of Generator Polynomials
  - Must be Prime binary number
  - The high and low order bits must be 1
  - CRC-8 : $X^8+X^2+X^1+1$
  - CRC-12: $X^{12}+X^{11}+X^3+X^2+1$
  - CRC-16 : $X^{16}+X^{15}+X^2+1$
  - CRC-CCITT:$X^{16}+X^{12}+X^5+1$
  - CRC-32 : $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X^1+1$
- Binary representation of CRC-16 =1 1000 0000 0000 0101

CRC Generator Implementation

Hardware implementation on polynomial division logic circuit can be implemented with two simple components:

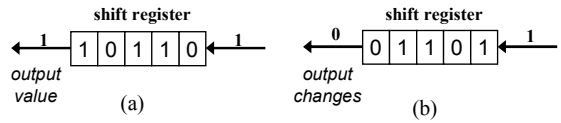
- ***An exclusive or (xor) unit***



(a)

	a	b	out
	0	0	0
	0	1	1
	1	0	1
(b)	1	1	0

- ***A shift register***



(a) (b)

CRC Generator Implementation

A shift register has two operations: ***initialize*** and ***shift.***

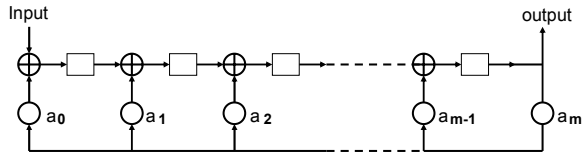
Initialize:

A shift register sets all bits to zero. As a result, its output also becomes zero.

Shift:

On coming clock pulse, the shift register instantaneously moves all bits to the left one position, sets the rightmost bit according to the current input, and sets the output according to the leftmost bit.

CRC Generator Implementation



The input is the polynomial to be divided. The output is the quotient and the remainder is contained in the shift register after all the input coefficients have been shifted into the generator. The receiver simply take the coded message and feed it into its generator for error check.

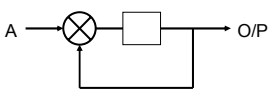
CRC Generator Implementation - Example

e.g. M(x)=[111]

G(x)=x+1

T(x)=[1110]

$$
\begin{array}{r}
101 \\
11 \overline{)\,1110} \\
\underline{11} \\
10 \\
\underline{11} \\
1
\end{array}
$$



A	Q	Q^+
1	0	1
1	1	0
1	0	1
0	1	

Further Reading

- Tanenbaum, Andrew, Computer Networks, 4th Ed.,, 2002.
- Pless, Vera, Introduction to the Theory of Error-Correcting Codes, 3rd Ed., 1998.
- Haykin, Simon, Communication Systems, 4th Ed., 2001.
- Proakis, John, Communication Systems Engineering, 2nd Ed., 2002.
- Bateman, Andy, Digital Communications, 1999.